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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,255	12/16/2004	Philippe Loyer	FR 020059	8333

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P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
ANDRAMUNO, FRANKLIN S	
ART UNIT	**PAPER NUMBER**
2623	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,255	LOYER, PHILIPPE	
	Examiner	Art Unit	
	Franklin S. Andramuno	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/16/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/16/04, 08/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bogot (US 2003/0086017 A1) in view of Walley (US Patent 6,114,888). Hereinafter referred as Bogot and Walley.

Regarding claim 1, Bogot discloses a converter apparatus for producing, from a first encoded signal supplied by a data source in a first encoding format at a first data rate **(A to B Reformatter (108) in figure 1B)**, a second signal encoded in a second encoding format at a second data rate **(B set-top box (110) in figure 1B)**, said converter apparatus comprising: decoding means for decoding the first encoded signal and for producing a decoded signal, encoding means for encoding said decoded signal into a second encoded signal **(Figure 2)**. **However, Bogot fails to specify** the use of a clock recovery along with clock loops and the use of oscillators for reconstructing the signal between analog and digital. Walley teaches the clock recovery **(figure 3)** means comprising an oscillator having a control frequency controlled by two complementary loops for producing a symbol clock for the encoding means **(Voltage controlled oscillator (213) in figure 2)**, which is locked on the first data rate **(Sample and hold (315) in figure 4)**, the two complementary loops including a coarse loop using a free

running reference clock and programmable dividing means for enabling the oscillator to reach a frequency which is close to a predetermined nominal frequency within a predefined tolerance range **(Loop Filter (309) in figure 3)**, and a fine loop using buffering means allowing control of the second data rate with respect to the first data rate by increasing/decreasing the oscillator-controlled frequency when the buffering means fills up/empties **(Loop gain Adjust (313) in figure 3)**, control means for controlling the decoding means, the encoding means and the coarse loop dividing means **(Duty Cycle and Gain adjust controller (325) in figure 3)**.

Therefore, it would have been obvious at the time of the invention modify Bogot's reference to include the use of clock recovery, Loop gains and loop filter along with an oscillator to change the signals between analog and digital. This is a useful combination because it allows the control of analog devices with digital signals produced by computers.

Regarding claim 2, Walley discloses a converter apparatus as claimed in claim 1, wherein the buffering means include a First Input First Output buffer having a current filling rate and which fills up at the first data rate and empties at the second data rate **(Noise Gating (329) in figure 3)**, the control frequency of the oscillator being controlled with respect to an estimation of a difference between the current filling rate and a predetermined nominal filling rate **(Duty Cycle and Gain Adjust Controller (325) in figure 3)**.

Regarding claim 3, Walley discloses a converter apparatus as claimed in claim 1, wherein the second data rate corresponds to a second symbol frequency **(Loop Gain**

Adjust (313) in figure 3), the symbol clock of the encoding means being a multiple of the second symbol frequency **(VCO (317) in figure 3)**.

Regarding claim 4, Bogot discloses a converter apparatus for producing, from a first encoded signal supplied by a data source in a first encoding format at a first data rate **(A to B Reformatter (108) in figure 1A)**, a second signal encoded in a second encoding format at a second data rate **(B Set-Top Box (110) in figure 1A)**, said converter apparatus comprising: decoding means for decoding the first encoded signal and for producing a decoded signal **(Demod (400) in figure 4)**, encoding means for encoding said decoded signal into a second encoded signal **(Mod (408) in figure 4)**, clock recovery means comprising an oscillator having a control frequency controlled by a control loop for producing a symbol clock for the encoding means **(Figure 3 Walley)**, which is locked on the first data rate, the control loop using buffering means allowing control of the second data rate with respect to the first data rate by increasing/decreasing the oscillator-controlled frequency when the buffering means fills up/empties **(Loop Gain Adjust (313) in figure 3 Walley)**, control means for controlling the decoding means, the encoding means and for forcing a nominal value into the oscillator corresponding to a nominal symbol clock rate for the encoding means **(Duty Cycle & Gain Adjust Controller (325) in figure 3 Walley)**.

3. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bogot (US 2003/0086017 A1) in view of Walley (US Patent 6,114,888) in view of

Lipsanen et al (US 2002/0059614 A1). Hereinafter referred as Bogot, Walley and Lipsanen.

Regarding claims 5-6, Bogot discloses a receiver for receiving a DVB-S signal encoded in the Satellite Digital Video Broadcasting format (DVB-S) **(DSS signal in figure 4)**, said receiver comprising a converter device for producing, from a received OFDM modulated DVB-T signal **(Mod (408) in figure 4)**, a QPSK modulated signal encoded in the Satellite Digital Video Broadcasting format (DVB-S) **(DVS-S signal in figure 4)**, said converter device comprising: demodulation means for demodulating the received OFDM modulated DVB-T signal and for providing a demodulated DVB-T signal **(Convert DSS CI Tables to DVB-SI and PSI Tables in figure 5)**, modulation means for re-modulating said demodulated DVB-T signal in an QPSK modulated signal **(Des Decryption (404) in figure 4)**, clock recovery means comprising an oscillator having a frequency controlled by two complementary loops **(Figure 3 in Walley)**. **However, Bogot and Walley fail to disclose the use of** QPSK for formatting the signals between DVB-T and DVB-S. Lipsanen discloses a system that provides a symbol clock for the QPSK modulator **(page 7 paragraph (0069))**, which is locked on the OFDM modulated DVB-T signal data rate, the two complementary loops including a coarse loop using a free running reference clock and programmable dividing means for enabling the oscillator to reach a frequency which is close to a predetermined nominal frequency within a predefined range **(Page 7 paragraph (0070)**, and a fine loop using buffering means allowing control of the data rate between the OFDM demodulator and the QPSK modulator by increasing/decreasing the oscillator controlled frequency when

the buffering means fills up/empties **(Page 4 paragraph (0042) lines 4-6)**, control means for controlling the demodulation means, the modulation means and the coarse loop dividing means **(Control (434) in figure 4)**.

Therefore it would have been obvious at the time of the invention to modify Bogot's reference to include the use of QPSK to modify the signals between DVB-T to DVB-S. This is a useful combination because it allows systems to exchange data between analog and digital devices. These devices can be anything from appliances at home to digital computer, stereos, video, etc.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Franklin S. Andramuno whose telephone number is 571-270-3004. The examiner can normally be reached on Mon-Thurs (7:30am - 5:00pm) alternate Fri off (EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on (571)272-7331. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600